PATENT APPLICATION

042390.P12399

Amendment

Amendment to Claims

Please amend the claims as shown below.

1. (Once amended) A memory device comprising:

an integrated circuit die including a memory array and having a first surface; and

a1 a voltage regulator circuit having a passive component, wherein the passive component is mounted overlying the first surface of the integrated circuit die and electrically coupled to the integrated circuit die, the voltage regulator circuit to provide a programming voltage potential to the memory array.

2. (Original) The memory device of claim 1, wherein the passive component is mounted to the integrated circuit die with an epoxy material.

3. (Original) The memory device of claim 2, wherein the epoxy material between the passive component and the integrated circuit die is less than about 0.050 millimeters in thickness.

4. (Original) The memory device of claim 1, wherein the passive component is mounted to the integrated circuit die with a conductive material.

5. (Original) The memory device of claim 1, wherein the passive component includes a capacitor or an inductor.

6. (Original) The memory device of claim 1, further comprising:

a substrate, wherein the integrated circuit die is mounted to the substrate.

a1 cont.

7. (Original) The memory device of claim 6, wherein the integrated circuit is mounted to the substrate with a non-conductive material.

8. (Original) The memory device of claim 6, further comprising a first wire bond electrically coupling at least a portion of the integrated circuit to the substrate.

9. (Original) The memory device of claim 8, further comprising a second wire bond electrically coupling at least a portion of the passive component to the substrate.

10. (Original) The memory device of claim 8, further comprising a second wire bond electrically coupling at least a portion of the passive component to the integrated circuit die.

11. (Original) The memory device of claim 1, wherein the integrated circuit die includes a flash memory array.

12. (Original) The memory device of claim 1, further comprising a voltage regulator coupled to the integrated circuit die, wherein at least a portion of the voltage regulator is mounted to the integrated circuit die.

13. (Once amended) A method comprising:

forming a substrate;

mounting an integrated circuit die on said substrate;

mounting at least a portion of a voltage regulator circuit having a passive component, the passive component mounted overlying the substrate; and

electrically coupling the passive component to at least a portion of the integrated circuit die.

14. (Original) The method of claim 13, further comprising adhesively attaching the passive component to the integrated circuit die.

15. (Original) The method of claim 14, further comprising adhesively attaching the passive component to the integrated circuit die with a non-conductive adhesive.

16. (Original) The method of claim 13 including wire bonding the passive component to the substrate.

17. (Original) The method of claim 13 including wire bonding the passive component to the integrated circuit die.

18. (Once amended) A method comprising:

molding an integrated circuit die and at least one passive component of a voltage regulator circuit into a package, the integrated circuit die including a non-volatile memory array, the voltage regulator circuit to provide a voltage potential to alter a state of a cell of the non-volatile memory array .

A1 cont.

19. (Original) The method of claim 18, further comprising mounting the at least one passive component to the integrated circuit die.

20. (Original) The method of claim 18, further comprising forming a wire bond to electrically couple the at least one passive component and the integrated circuit.